REMARKS

Reconsideration of this application, as presently amended, is respectfully requested. Claims 1-20 are pending in this application. Claims 16 and 20 stand rejected. Claims 1-12 are withdrawn from consideration as being directed to a non-elected invention. Claims 13-15 and 17-19 are allowed.

Request for Telephonic Interview

In the RCE filed on August 4, 2006, claims 16 and 20 were amended to clarify the invention from the cited prior art based on comments made by the Examiner and her supervisor during a personal interview conducted on July 25, 2006. However, the rejection set forth in the Office Action mailed October 17, 2006 has not provided a specific response to the patentablity arguments submitted with the RCE filed on August 4, 2006. Instead, the Office Action quotes the present claim language and cites the same elements shown in applicant's Fig. 16 as were cited in the previous Office Actions.

In view of the fact that the amendments submitted with the Request for Continued Examination (RCE) filed on August 4, 2006 were made to clarify the invention based on comments made by the Examiner and her supervisor during the personal interview conducted on July 25, 2006, if the Examiner believes the current rejection still has merit, applicant respectfully requests that the Examiner contact the undersigned attorney to further discuss the rejection prior to issuing a subsequent Office Action.

Claim Rejection – 35 U.S.C. §102

Claims 16 and 20 are rejected under 35 U.S.C. §102(a) as being anticipated by Applicant's admitted prior art (**AAPA**) Fig. 16. For the reasons set forth in detail below, this rejection is respectfully traversed.

Initially, it is noted that claims 16 and 20 have been amended to further clarify the invention by reciting "an arithmetic circuit ~~multiplying~~ that receives said matrix produced by the logic circuit as an input, multiplies said predetermined initial values stored in said storage circuit by said matrix produced by said logic circuit to compute a value of each code forming said sequence of scrambling codes, and outputs said sequence of scrambling codes".

This proposed amendment is intended to make clear that the claimed arithmetic circuit ***receives the matrix produced by the logic circuit as an input*** and ***outputs the sequence of scrambling codes***. It is believed that the amended claims make clear that the claimed arithmetic circuit (corresponding to the arithmetic circuit 28d of the embodiment shown in Fig. 13) receives as an input the matrix produced by the claimed logic circuit (corresponding to the elements 28a, 28b, 28c shown in Fig. 13) and multiplies the initial value (of the initial value buffer 22) by the matrix to output the scrambling code sequence. As will be discussed in detail below, the arithmetic circuit 21 of Fig. 16 does not receive a matrix from the logic circuit (shift registers 11-14) as an input, and does not output the sequence of scrambling codes.

In the RCE filed on August 4, 2006, claims 16 and 20 were amended to recite that the claimed "logic circuit" ***produces a matrix*** and the claimed "arithmetic circuit" multiplies the predetermined initial values by the ***matrix produced by the logic circuit***. Further, it was argued

that, in contrast to the claimed invention, the matrices ***produced*** by the logic circuit shown in Fig. 16 (considered by the Examiner to correspond to shift registers 11, 12, 13 and 14 in Fig. 16) are **not** used by the arithmetic circuit (considered by the Examiner to correspond to the arithmetic circuit 21 in Fig. 16) for multiplication with the predetermined initial values Ri.

Although the Examiner has not provided any specific response to the patentability arguments submitted with the RCE filed on August 4, 2006, based on the current rejection, it appears that the Examiner believes that the matrices $M_{0(100)}$-$M_{3(100)}$ used by the arithmetic circuit 21 are ***produced*** **by operations of the shift registers 11-14** (considered by the Examiner to be the logic circuit). *More specifically, in the final paragraph on page 2 of the Office Action, the Examiner asserts that the matrices* $M_{0(100)}$-$M_{3(100)}$ *are produced after "100 operations of the* ***shift register****".*

It is respectfully submitted that it is clear from the disclosure of the present application that the matrices $M_{0(100)}$-$M_{3(100)}$ are ***not produced by operations of the shift registers 11-14***. More specifically, as shown in Fig. 16, the only connection between the arithmetic circuit 21 and the shift registers 11-14 is through selectors 15-18. The selectors 15-18 do ***not provide inputs to the arithmetic circuit 21***. More specifically, the selectors 15-18 select between two input values, one of which is a value R_{o3}, R_{o2}, R_{o1}, R_{o0} input from arithmetic circuit 21 (see page 10, lines 3-4 of present application). The selectors 15-18 do ***not produce matrices*** $M_{0(100)}$-$M_{3(100)}$ that are input to the arithmetic circuit 21. Thus, it is clear that, contrary to the Examiner's assertion, the matrices $M_{0(100)}$-$M_{3(100)}$ that are multiplied by the predetermined initial values R_i by the arithmetic circuit 21 are ***not produced*** by the logic circuit (shift registers 11-14).

Further, applicant's specification discloses that matrices $M_{3(100)}$, $M_{2(100)}$, $M_{1(100)}$, $M_{0(100)}$ used by arithmetic circuit 21 are ***stored in advance*** in a memory or register (see page 9, lines 8-10 and lines 21-23 of applicant's specification), or that the ***arithmetic circuit 21 itself generates the matrices*** $M_{3(100)}$ - $M_{0(100)}$ (see page 9, lines 24-25 of applicant's specification). However, applicant's specification does not disclose or suggest that the matrices stored therein are produced by the shift registers 11-14 (logic circuit).

Still further, it is clear from Fig. 16 that the arithmetic circuit 21 computes values Ro_3, Ro_2, Ro_1 and Ro_0 that are supplied to the selectors 15-18 (of the logic circuit). However, the values Ro_3, Ro_2, Ro_1 and Ro_0 are not codes forming a sequence of scrambling codes. Rather, the values Ro_3, Ro_2, Ro_1 and Ro_0 are initial values of registers 11-14 after one hundred (100) shift operations (see page 10, lines 1-2 of applicant's specification). The sequence of scrambling codes is generated by additional shift operations subsequent to the loading the values representing the shift operation of 100 times (see page 10, lines 4-9 of applicant's specification).

Therefore, unlike the claimed invention, the arithmetic circuit 21 shown in Fig. 16 of applicant's specification does not "*[multiply] said predetermined initial values stored in said storage circuit by said matrix produced by said logic circuit* ***to compute a value of each code forming said sequence of scrambling codes***". As described above, the values Ro_3, Ro_2, Ro_1 and Ro_0 output by the arithmetic circuit 21 are initial values of registers 11-14 after one hundred (100) shift operations. However, the sequence of scrambling codes is generated ***by additional shift operations subsequent to the loading the values representing the shift operation of 100 times*** (see page 10, lines 4-9 of applicant's specification). Thus, unlike the claimed invention,

the arithmetic circuit 21 does not compute a value of each code forming said sequence of scrambling codes.

Accordingly, in view of the above amendments and remarks, it is respectfully submitted that claims 16 and 20 patentably distinguish over the cited prior art. Reconsideration and withdrawal of the rejection under §102 are respectfully requested.

CONCLUSION

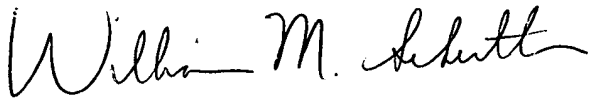
In view of the foregoing amendments and accompanying remarks, it is submitted that all pending claims are in condition for allowance. A prompt and favorable reconsideration of the rejection and an indication of allowability of all pending claims are earnestly solicited.

If the Examiner believes that there are issues remaining to be resolved in this application, the Examiner is invited to contact the undersigned attorney at the telephone number indicated below to arrange for an interview to expedite and complete prosecution of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



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